

High Performance 2A and 3A Linear Regulators

ISL80102, ISL80103

The ISL80102 and ISL80103 are low voltage, high-current, single output LDOs specified for 2A and 3A output current, respectively. These LDOs operate from input voltages of 2.2V to 6V and are capable of providing output voltages of 0.8V to 5V on the adjustable V_{OUT} versions. Fixed output voltage options are available in 1.5V, 1.8V, 2.5V, 3.3V and 5V. Other custom voltage options available upon request.

For applications that demand in-rush current less than the current limit, an external capacitor on the soft start pin provides adjustment. The ENABLE feature allows the part to be placed into a low quiescent current shutdown mode. A sub-micron BiCMOS process is utilized for this product family to deliver the best in class analog performance and overall value.

These CMOS LDOs will consume significantly lower quiescent current as a function of load over bipolar LDOs, which translates into higher efficiency and the ability to consider packages with smaller footprints. Quiescent current is modestly compromised to enable a leading class fast load transient response, and hence a lower total AC regulation band for an LDO in this category.

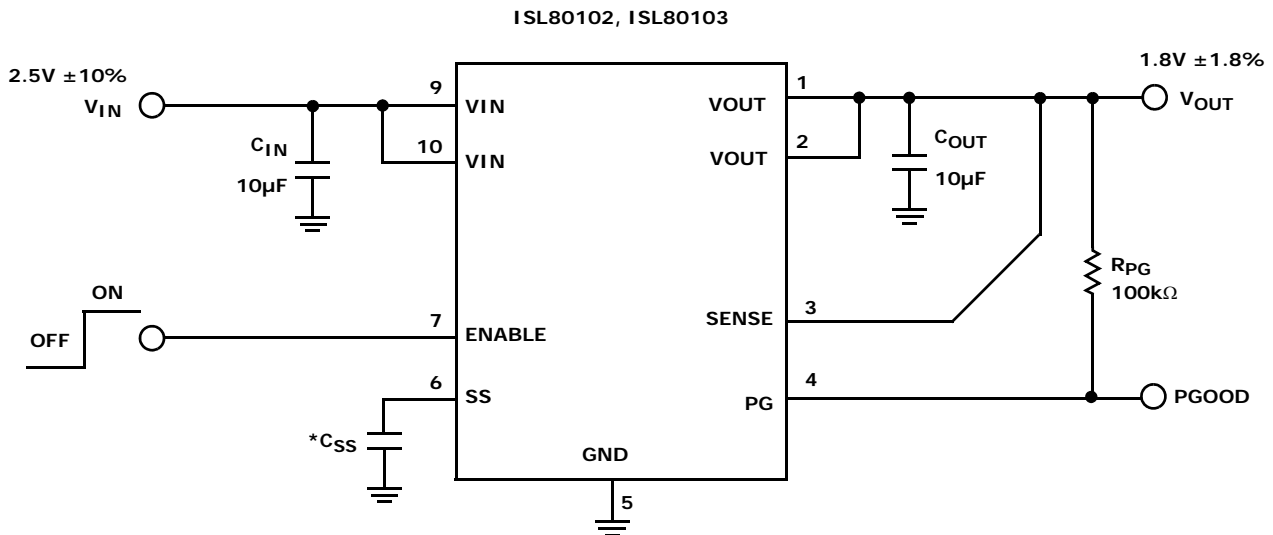
Features

- Stable with all Capacitor Types (Note 11)
- 2A and 3A Output Current Ratings
- 2.2V to 6V Input Voltage Range
- $\pm 1.8\%$ V_{OUT} Accuracy Guaranteed Over Line, Load and $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$
- Very Low 120mV Dropout Voltage at 3A (ISL80103)
- Fixed and Adjustable V_{OUT} Versions
- Very Fast Transient Response
- Excellent 62dB PSRR
- $100\mu\text{V}_{\text{RMS}}$ Output Noise
- Power-Good Output
- Adjustable In-Rush Current Limiting
- Short Circuit and Over-Temperature Protection
- Available in a 10 Ld DFN (now), 5Ld TO220 and 5Ld TO263 (soon)

Applications* (see page 14)

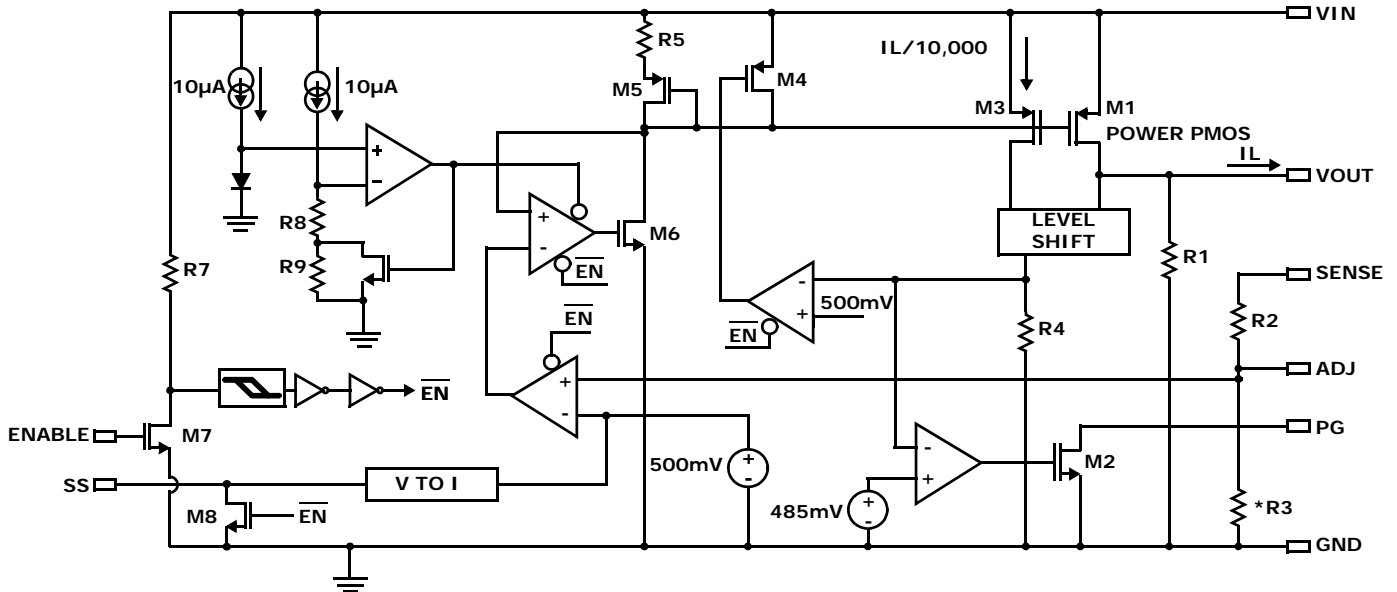
- Servers
- Telecommunications and Networking
- Medical Equipment
- Instrumentation Systems
- Routers and Switchers

Typical Application



*CSS is optional, (see Note 12) on page 5.

Block Diagram



*R3 is open for ADJ versions.

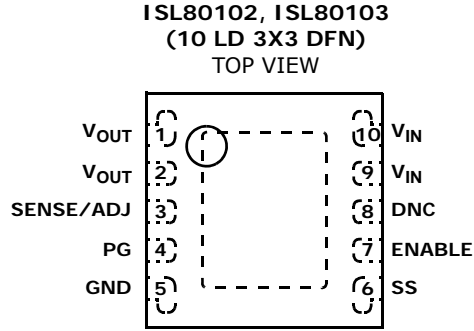
Ordering Information

PART NUMBER (Notes 1, 2, 4)	PART MARKING	V _{OUT} VOLTAGE	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG DWG. #
ISL80102IRAJZ	DZJA	ADJ	-40 to +125	10 Ld 3x3 DFN	L10.3x3
ISL80102IR15Z	DZMA	1.5V (Note 3)	-40 to +125	10 Ld 3x3 DFN	L10.3x3
ISL80102IR18Z	DZNA	1.8V	-40 to +125	10 Ld 3x3 DFN	L10.3x3
ISL80102IR25Z	DZPA	2.5V	-40 to +125	10 Ld 3x3 DFN	L10.3x3
ISL80102IR33Z	DZRA	3.3V (Note 3)	-40 to +125	10 Ld 3x3 DFN	L10.3x3
ISL80102IR50Z	DZSA	5.0V (Note 3)	-40 to +125	10 Ld 3x3 DFN	L10.3x3
ISL80103IRAJZ	DZAA	ADJ	-40 to +125	10 Ld 3x3 DFN	L10.3x3
ISL80103IR15Z	DZDA	1.5V (Note 3)	-40 to +125	10 Ld 3x3 DFN	L10.3x3
ISL80103IR18Z	DZEA	1.8V	-40 to +125	10 Ld 3x3 DFN	L10.3x3
ISL80103IR25Z	DZFPA	2.5V	-40 to +125	10 Ld 3x3 DFN	L10.3x3
ISL80103IR33Z	DZGA	3.3V (Note 3)	-40 to +125	10 Ld 3x3 DFN	L10.3x3
ISL80103IR50Z	DZHA	5.0V (Note 3)	-40 to +125	10 Ld 3x3 DFN	L10.3x3

NOTES:

1. Add "-T" or "-TK" suffix for tape and reel. Please refer to [TB347](#) for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. The 1.5V, 3.3V and 5V fixed output voltages will be released in the future. Please contact Intersil Marketing for more details.
4. For Moisture Sensitivity Level (MSL), please see device information page for [ISL80102](#), [ISL80103](#). For more information on MSL please see tech brief [TB363](#).

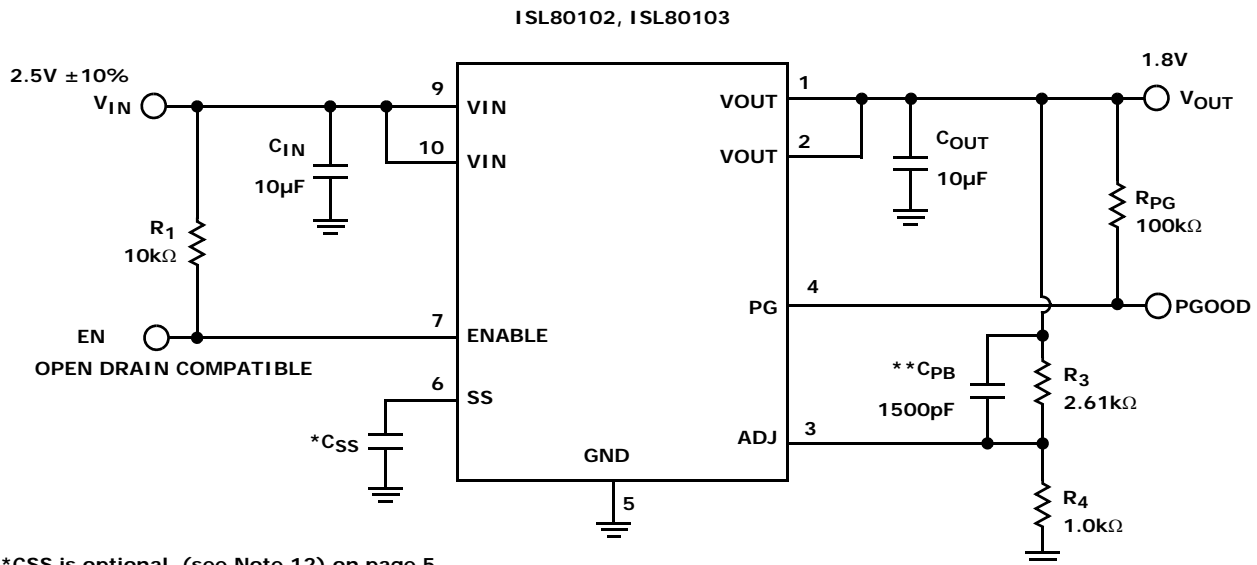
Pin Configuration



Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
1, 2	V _{OUT}	Output voltage pin.
3	SENSE/ADJ	Remote voltage sense for internally fixed V _{OUT} options. ADJ pin for externally set V _{OUT} .
4	PG	V _{OUT} in regulation signal. Logic low defines when V _{OUT} is not in regulation. Must be grounded if not used.
5	GND	GND pin.
6	SS	External cap adjusts in-rush current.
7	ENABLE	V _{IN} independent chip enable. TTL and CMOS compatible.
8	DNC	Do not connect this pin to ground or supply. Leave floating.
9, 10	V _{IN}	Input supply pin.
	EPAD	EPAD at ground potential. Soldering it directly to GND plane is optional.

Typical Application



*C_{SS} is optional, (See Note 12) on page 5.

**C_{PB} is optional. See "Functional Description" on page 12 for more information.

FIGURE 1. TYPICAL APPLICATION DIAGRAM

ISL80102, ISL80103

Absolute Maximum Ratings (Note 7)

V_{IN} relative to GND	-0.3V to +6.5V
V_{OUT} relative to GND	-0.3V to +6.5V
PG, ENABLE, SENSE/ADJ, SS	
Relative to GND	-0.3V to +6.5V

Recommended Operating Conditions

(Note 10)

Junction Temperature Range (T_J)	-40°C to +125°C
V_{IN} relative to GND	2.2V to 6V
V_{OUT} range	.800mV to 5V
PG, ENABLE, SENSE/ADJ, SS relative to GND	0V to 6V
PG sink current	10mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
10 Ld 3x3 DFN Package (Notes 5, 6)	48	4
Maximum Junction Temperature (Plastic Package)	+150°C	
Storage Temperature Range	-65°C to +150°C	
Pb-Free Reflow Profile	see link below	
	http://www.intersil.com/pbfree/Pb-FreeReflow.asp	

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

- θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
- For θ_{JC} , the "case temp" location is the center of the exposed metal pad on the package underside.
- ABS max voltage rating is defined as the voltage applied for a lifetime average duty cycle above 6V of 1%.

Electrical Specifications

Unless otherwise noted, all parameters are established over the following specified conditions: $V_{IN} = V_{OUT} + 0.4V$, $V_{OUT} = 1.8V$, $C_{IN} = C_{OUT} = 10\mu F$, $T_J = +25^\circ C$, $I_{LOAD} = 0A$. Applications must follow thermal guidelines of the package to determine worst case junction temperature. Please refer to "Functional Description" on page 12 and Tech Brief [TB379](#). **Boldface limits apply over the operating temperature range, -40°C to +125°C.** Pulse load techniques used by ATE to ensure $T_J = T_A$ defines established limits.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
DC CHARACTERISTICS						
DC Output Voltage Accuracy	V_{OUT}	V_{OUT} Options: 1.8V. $V_{IN} = 2.2V$; $I_{LOAD} = 0A$		0.5		%
		V_{OUT} Options: 1.8V. $2.2V < V_{IN} < 3.6V$; $0A < I_{LOAD} < 3A$	-1.8		1.8	%
		V_{OUT} Options: 2.5V $V_{IN} = V_{OUT} + 0.4V$; $I_{LOAD} = 0A$		0.5		%
		V_{OUT} Options: 2.5V $V_{OUT} + 0.4V < V_{IN} < 6V$; $0A < I_{LOAD} < 3A$	-1.8		-1.8	%
Feedback Pin (ADJ Version)	V_{FB}	$2.2V < V_{IN} < 6V$, $0A < I_{LOAD} < 3A$	491	500	509	mV
DC Input Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	$V_{OUT} + 0.4V < V_{IN} < 3.6V$, $V_{OUT} = 1.8V$		0.1	0.4	%
		$V_{OUT} + 0.4V < V_{IN} < 6V$, $V_{OUT} = 2.5V$		0.1	0.8	%
DC Output Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	$0A < I_{LOAD} < 3A$, All voltage options	-0.8			%
		$0A < I_{LOAD} < 2A$, All voltage options	-0.6			%
Feedback Input Current		$V_{ADJ} = 0.5V$		0.01	1	μA
Ground Pin Current	I_Q	$I_{LOAD} = 0A$, $2.2V < V_{IN} < 6V$		7.5	9	mA
		$I_{LOAD} = 3A$, $2.2V < V_{IN} < 6V$		8.5	12	mA
Ground Pin Current in Shutdown	I_{SHDN}	ENABLE Pin = 0.2V, $V_{IN} = 5V$		0.4		μA
		ENABLE Pin = 0.2V, $V_{IN} = 6V$		3.3	16	μA
Dropout Voltage (Note 9)	V_{DO}	$I_{LOAD} = 3A$, $V_{OUT} = 2.5V$, 10 LD 3x3 DFN		120	185	mV
		$I_{LOAD} = 2A$, $V_{OUT} = 2.5V$, 10 LD 3x3 DFN		81	125	mV

ISL80102, ISL80103

Electrical Specifications Unless otherwise noted, all parameters are established over the following specified conditions: $V_{IN} = V_{OUT} + 0.4V$, $V_{OUT} = 1.8V$, $C_{IN} = C_{OUT} = 10\mu F$, $T_J = +25^\circ C$, $I_{LOAD} = 0A$. Applications must follow thermal guidelines of the package to determine worst case junction temperature. Please refer to "Functional Description" on page 12 and Tech Brief [TB379](#). **Boldface limits apply over the operating temperature range, $-40^\circ C$ to $+125^\circ C$.** Pulse load techniques used by ATE to ensure $T_J = T_A$ defines established limits.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
Output Short Circuit Current (3A Version)	ISC	$V_{OUT} = 0V, V_{OUT} + 0.4V < V_{IN} < 6V$		5.0		A
Output Short Circuit Current (2A Version)		$V_{OUT} = 0V, V_{OUT} + 0.4V < V_{IN} < 6V$		2.8		A
Thermal Shutdown Temperature	TSD	$V_{OUT} + 0.4V < V_{IN} < 6V$		160		$^\circ C$
Thermal Shutdown Hysteresis (Rising Threshold)	TSDn	$V_{OUT} + 0.4V < V_{IN} < 6V$		15		$^\circ C$
AC CHARACTERISTICS						
Input Supply Ripple Rejection	PSRR	$f = 1kHz, I_{LOAD} = 1A; V_{IN} = 2.2V$		55		dB
		$f = 120Hz, I_{LOAD} = 1A; V_{IN} = 2.2V$		62		
Output Noise Voltage		$I_{LOAD} = 10mA, BW = 300Hz < f < 300kHz$		100		μV_{RMS}
ENABLE PIN CHARACTERISTICS						
Turn-on Threshold	$V_{EN(HIGH)}$	$2.2V < V_{IN} < 6V$	0.3	0.8	0.95	V
Hysteresis (Rising Threshold)	$V_{EN(HYS)}$	$2.2V < V_{IN} < 6V$		135		mV
Enable Pin Turn-on Delay	t_{EN}	$C_{OUT} = 10\mu F, I_{LOAD} = 1A$		150		μs
Enable Pin Leakage Current		$V_{IN} = 6V, EN = 3V$			1	μA
SOFT-START CHARACTERISTICS						
Reset Pull-Down resistance	R_{PD}			323		Ω
Soft Start Charge Current	I_{CHG}		-7	-4.5	-2	μA
PG PIN CHARACTERISTICS						
V_{OUT} PG Flag Threshold			75	84	92	$\%V_{OUT}$
V_{OUT} PG Flag Hysteresis				4		%
PG Flag Low Voltage		$I_{SINK} = 500\mu A$		47	100	mV
PG Flag Leakage Current		$V_{IN} = 6V, PG = 6V$		0.05	1	μA

NOTES:

- Parameters with MIN and/or MAX limits are 100% tested at $+25^\circ C$, unless otherwise specified. Temperature limits established by characterization and are not production tested.
- Dropout is defined by the difference in supply V_{IN} and V_{OUT} when the supply produces a 2% drop in V_{OUT} from its nominal value.
- Electromigration specification defined as lifetime average junction temperature of $+110^\circ C$ where max rated DC current = lifetime average current.
- Minimum cap of $10\mu F$ X5R/X7R on V_{IN} and V_{OUT} required for stability.
- If the current limit for in-rush current is acceptable in application, do not use this feature. Used only when large bulk capacitance required on V_{OUT} for application.

Typical Operating Performance

Unless otherwise noted: $V_{IN} = 2.2V$, $V_{OUT} = 1.8V$, $C_{IN} = C_{OUT} = 10\mu F$, $T_J = +25^\circ C$, $I_L = 0A$.

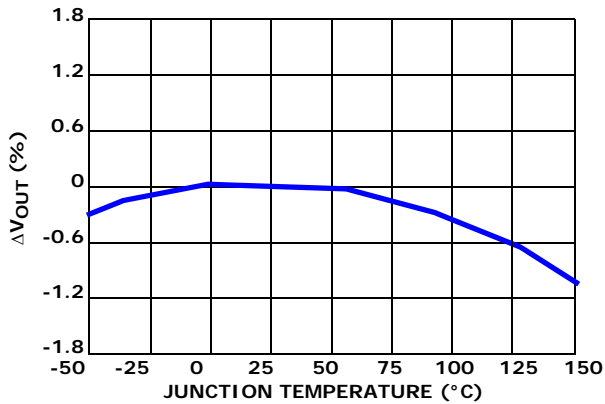


FIGURE 2. ΔV_{OUT} vs TEMPERATURE

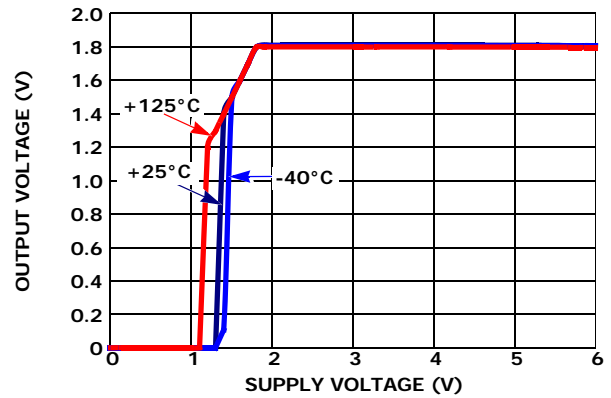


FIGURE 3. OUTPUT VOLTAGE vs SUPPLY VOLTAGE

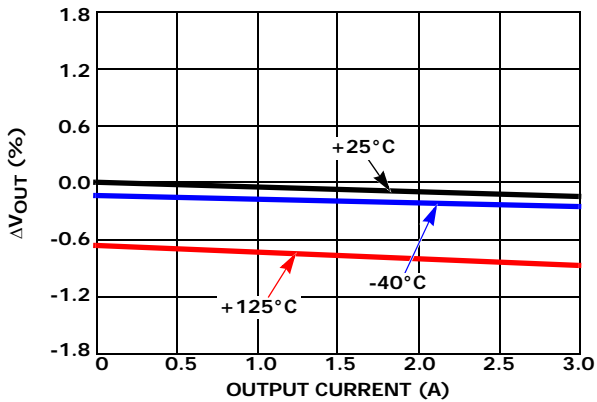


FIGURE 4. ΔV_{OUT} vs OUTPUT CURRENT

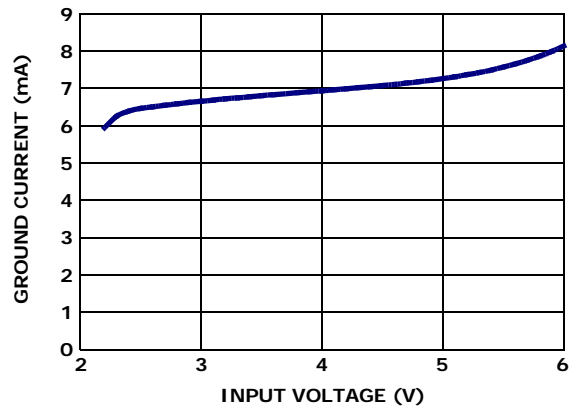


FIGURE 5. GROUND CURRENT vs SUPPLY VOLTAGE

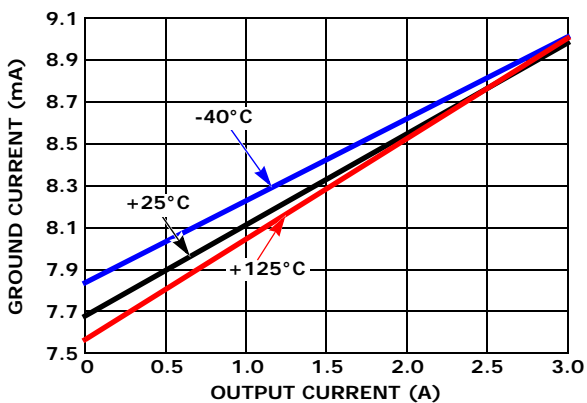


FIGURE 6. GROUND CURRENT vs OUTPUT CURRENT

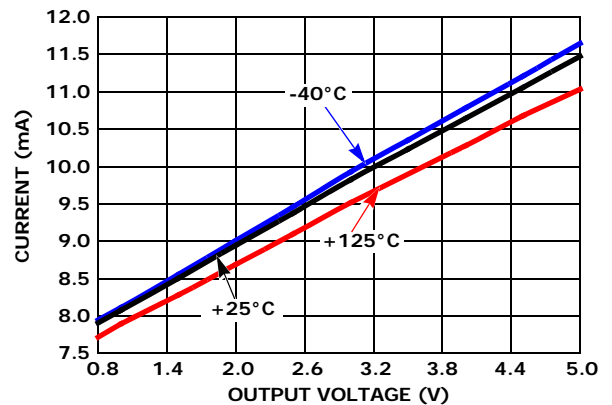


FIGURE 7. GROUND CURRENT vs OUTPUT VOLTAGE

Typical Operating Performance

Unless otherwise noted: $V_{IN} = 2.2V$, $V_{OUT} = 1.8V$, $C_{IN} = C_{OUT} = 10\mu F$, $T_J = +25^\circ C$, $I_L = 0A$. (Continued)

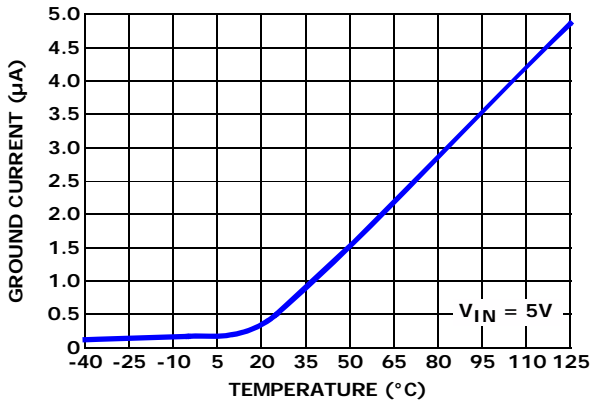


FIGURE 8. SHUTDOWN CURRENT vs TEMPERATURE

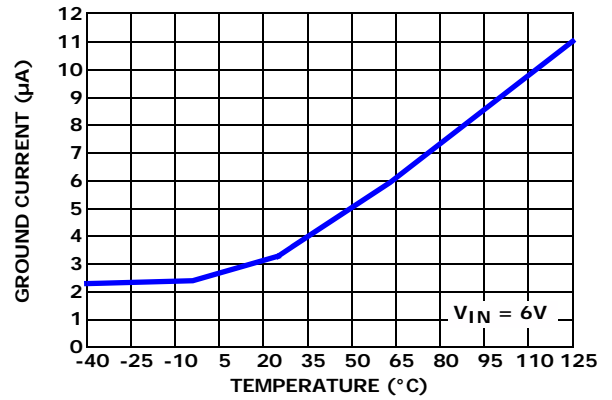


FIGURE 9. SHUTDOWN CURRENT vs TEMPERATURE

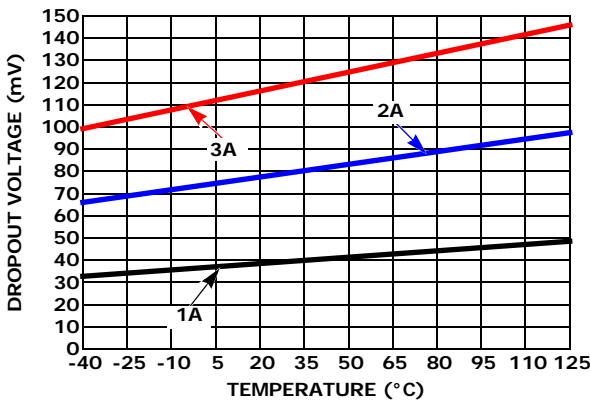


FIGURE 10. DROPOUT VOLTAGE vs TEMPERATURE

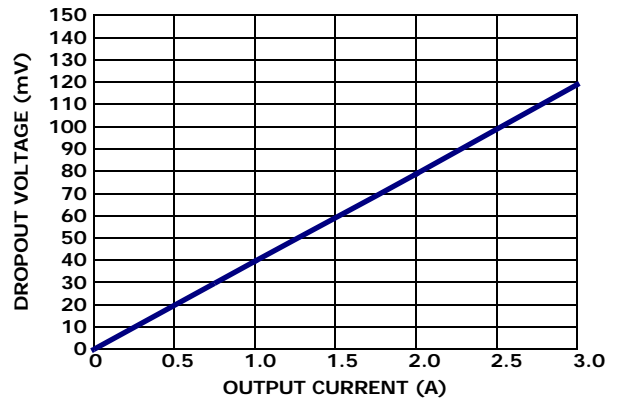


FIGURE 11. DROPOUT VOLTAGE vs OUTPUT CURRENT

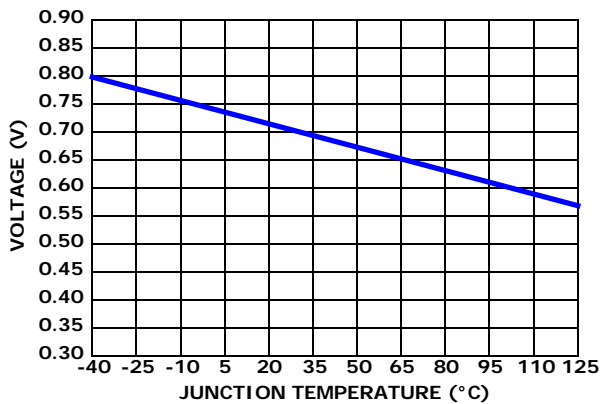


FIGURE 12. ENABLE THRESHOLD VOLTAGE vs TEMPERATURE

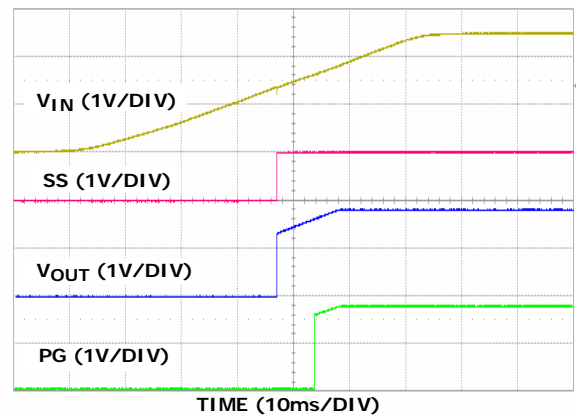


FIGURE 13. POWER-UP ($V_{IN} = 2.2V$)

Typical Operating Performance

Unless otherwise noted: $V_{IN} = 2.2V$, $V_{OUT} = 1.8V$, $C_{IN} = C_{OUT} = 10\mu F$, $T_J = +25^\circ C$, $I_L = 0A$. (Continued)

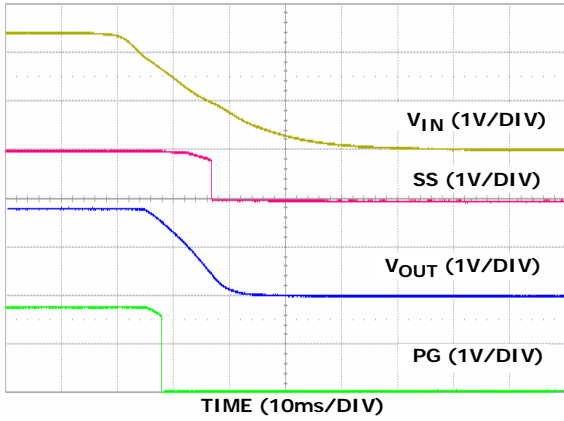


FIGURE 14. POWER-DOWN ($V_{IN} = 2.2V$)

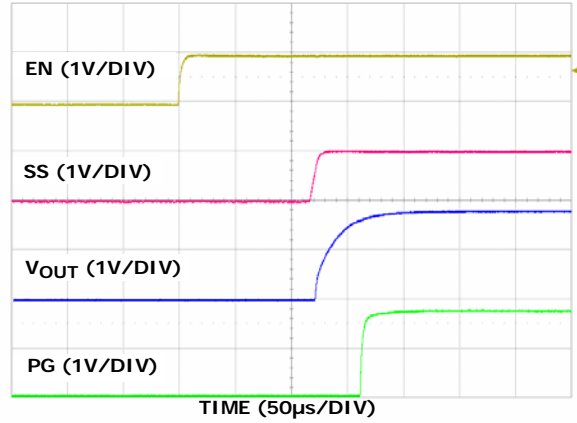


FIGURE 15. ENABLE START-UP

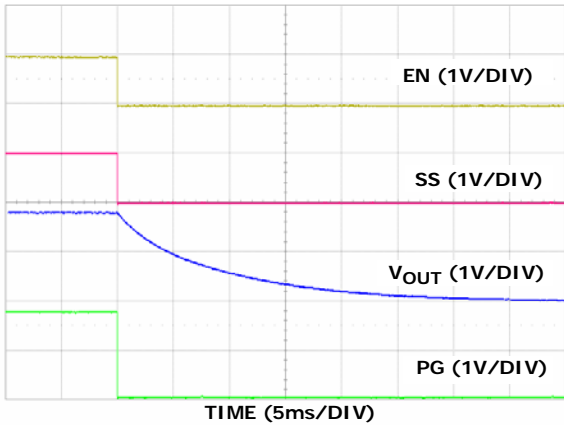


FIGURE 16. ENABLE SHUTDOWN

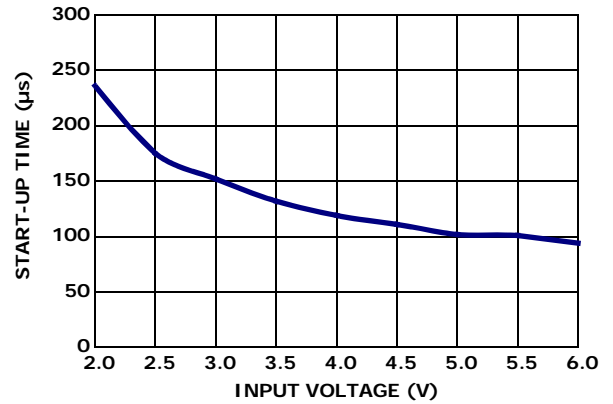


FIGURE 17. START-UP TIME vs SUPPLY VOLTAGE

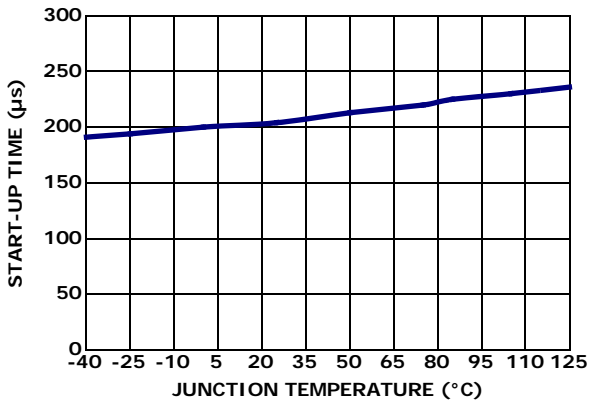


FIGURE 18. START-UP TIME vs TEMPERATURE

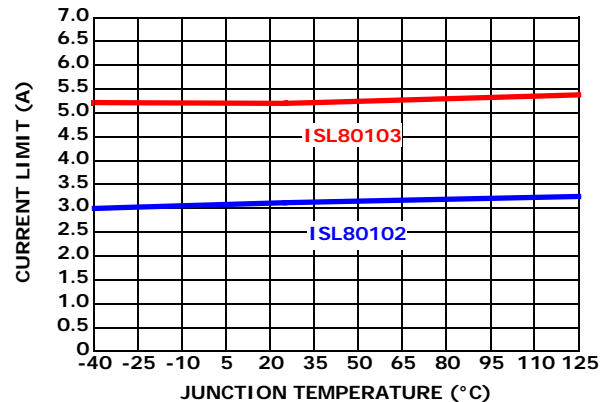


FIGURE 19. CURRENT LIMIT vs TEMPERATURE

Typical Operating Performance

Unless otherwise noted: $V_{IN} = 2.2V$, $V_{OUT} = 1.8V$, $C_{IN} = C_{OUT} = 10\mu F$, $T_J = +25^\circ C$, $I_L = 0A$. (Continued)

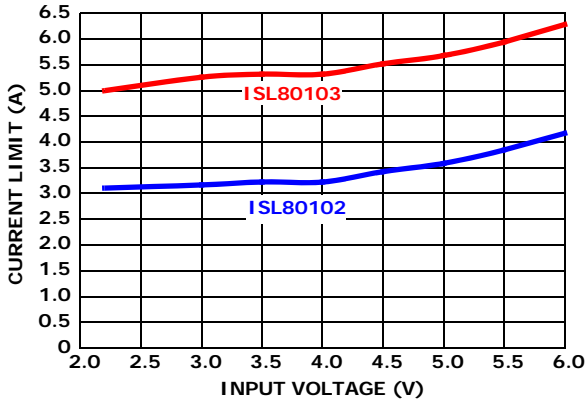


FIGURE 20. CURRENT LIMIT vs SUPPLY VOLTAGE

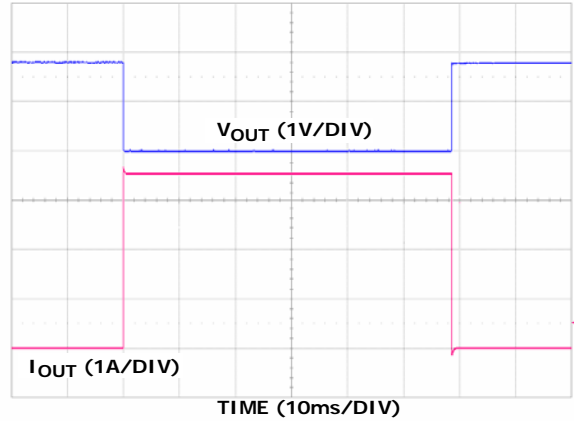


FIGURE 21. CURRENT LIMIT RESPONSE (ISL80102)

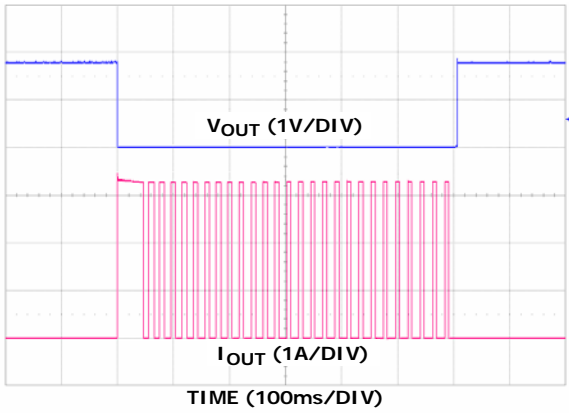


FIGURE 22. THERMAL CYCLING (ISL80102)

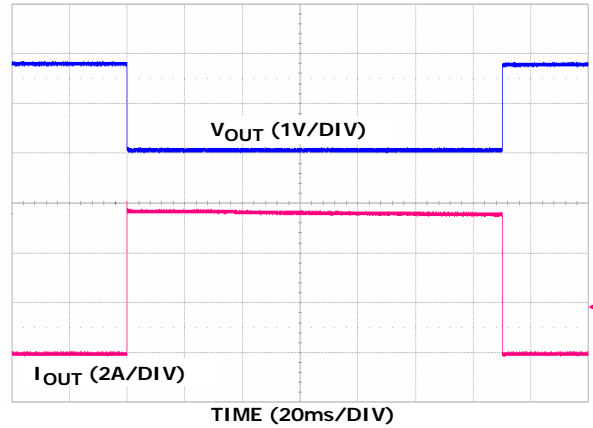


FIGURE 23. CURRENT LIMIT RESPONSE (ISL80103)

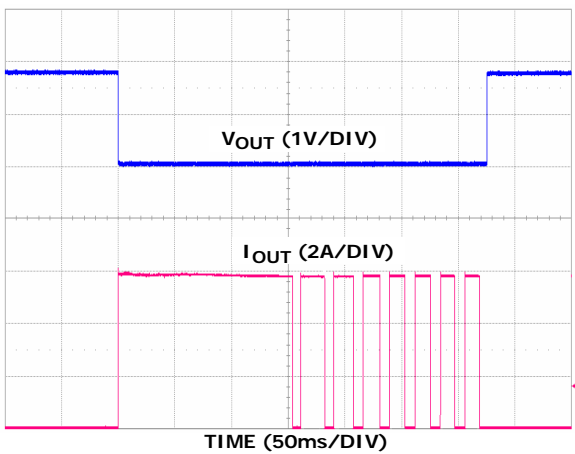


FIGURE 24. THERMAL CYCLING (ISL80103)

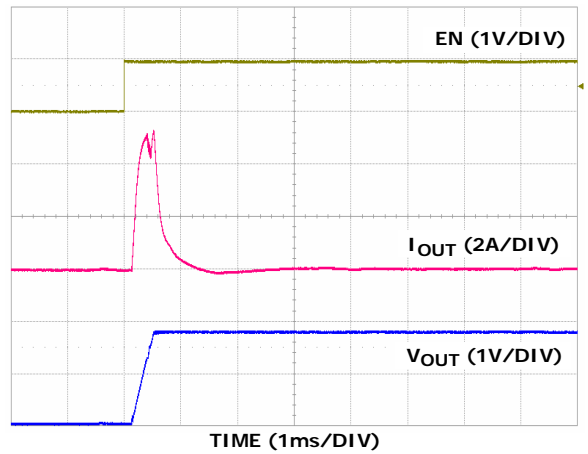


FIGURE 25. IN-RUSH CURRENT WITH NO SOFT-START CAPACITOR, $C_{OUT} = 1000\mu F$

Typical Operating Performance

Unless otherwise noted: $V_{IN} = 2.2V$, $V_{OUT} = 1.8V$, $C_{IN} = C_{OUT} = 10\mu F$, $T_J = +25^\circ C$, $I_L = 0A$. (Continued)

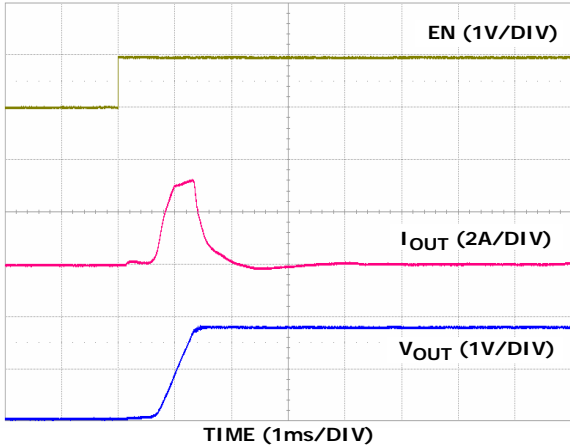


FIGURE 26. IN-RUSH WITH 22nF SOFT-START CAPACITOR, $C_{OUT} = 1000\mu F$

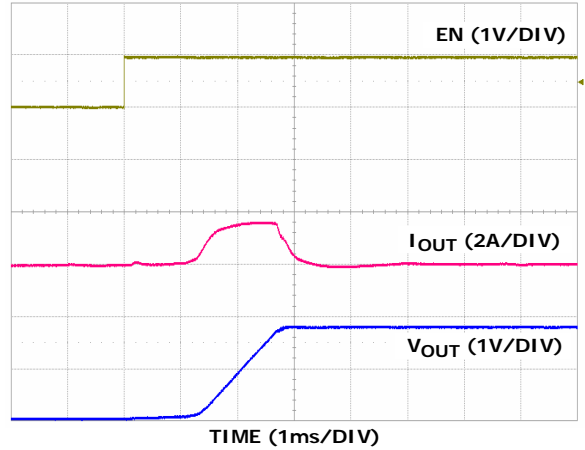


FIGURE 27. IN-RUSH WITH 47nF SOFT-START CAPACITOR, $C_{OUT} = 1000\mu F$

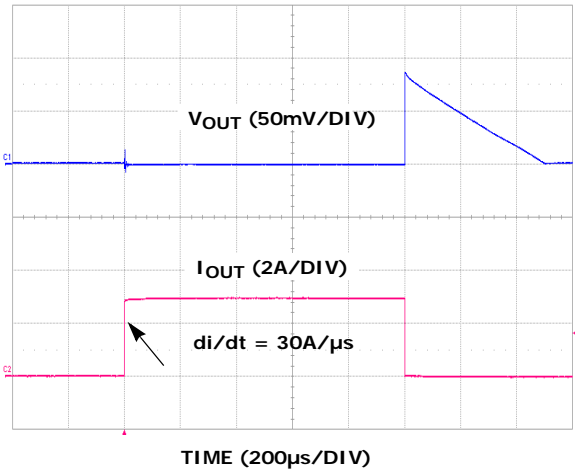


FIGURE 28. LOAD TRANSIENT 0A TO 3A, $C_{OUT} = 10\mu F$ CERAMIC

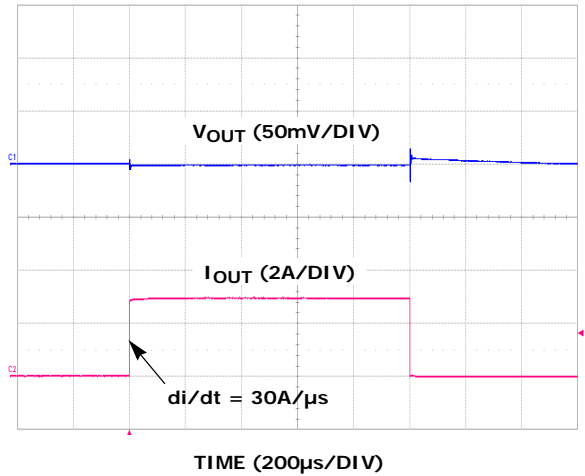


FIGURE 29. LOAD TRANSIENT 0A TO 3A, $C_{OUT} = 10\mu F$ CERAMIC + $100\mu F$ OSCON

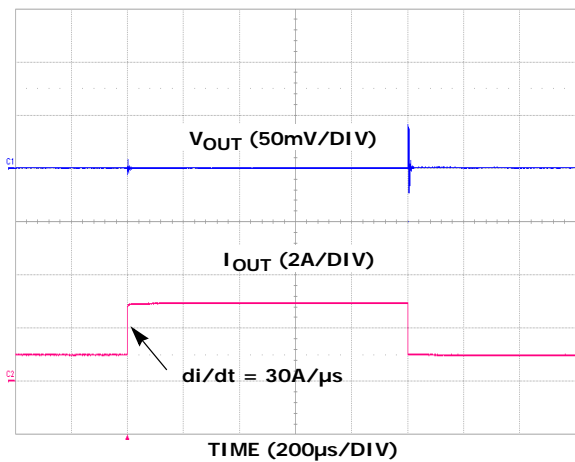


FIGURE 30. LOAD TRANSIENT 1A TO 3A, $C_{OUT} = 10\mu F$ CERAMIC

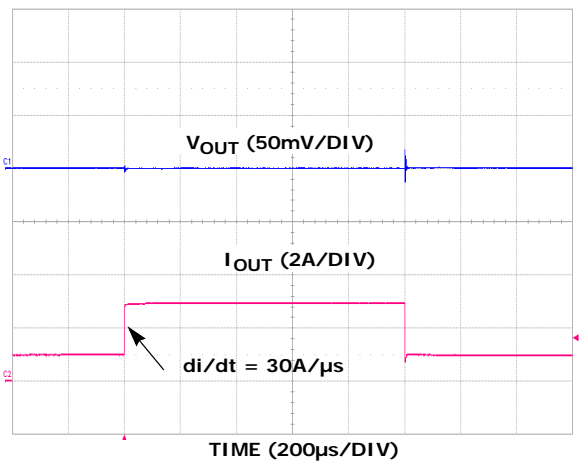


FIGURE 31. LOAD TRANSIENT 1A TO 3A, $C_{OUT} = 10\mu F$ CERAMIC + $100\mu F$ OSCON

Typical Operating Performance

Unless otherwise noted: $V_{IN} = 2.2V$, $V_{OUT} = 1.8V$, $C_{IN} = C_{OUT} = 10\mu F$, $T_J = +25^\circ C$, $I_L = 0A$. (Continued)

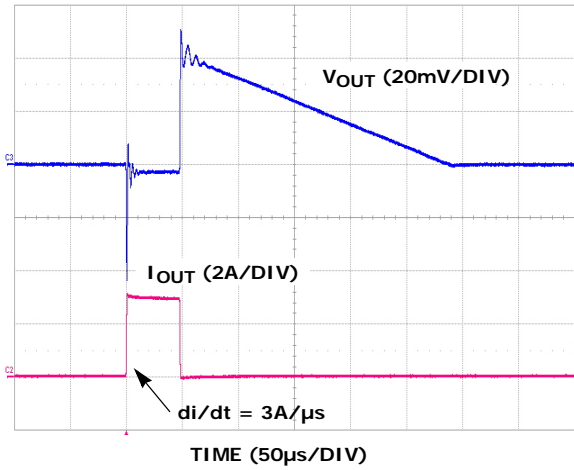


FIGURE 32. LOAD TRANSIENT 0A TO 3A, $C_{OUT} = 10\mu F$ CERAMIC, No C_{PB} (ADJ VERSION)

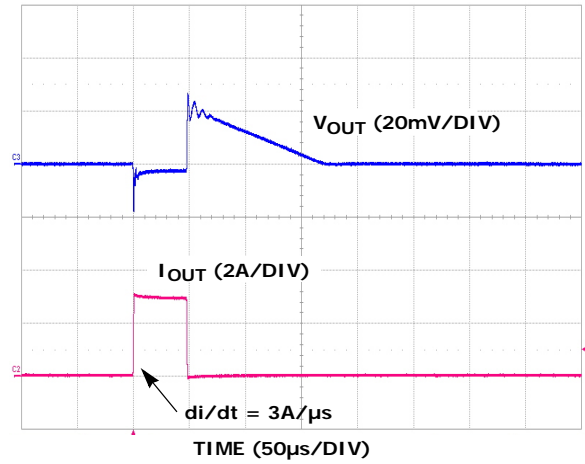


FIGURE 33. LOAD TRANSIENT 0A TO 3A, $C_{OUT} = 10\mu F$ CERAMIC, $C_{PB} = 150pF$ (ADJ VERSION)

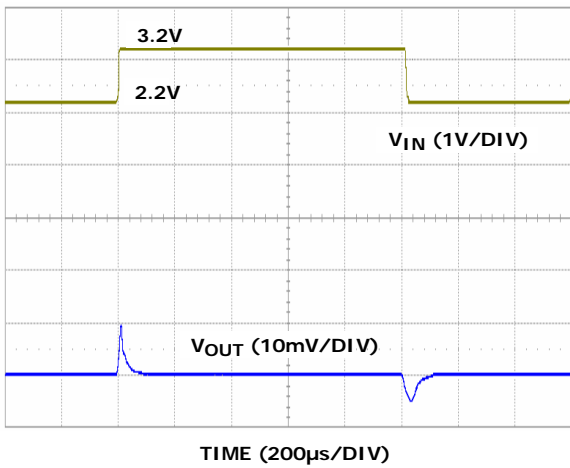


FIGURE 34. LINE TRANSIENT

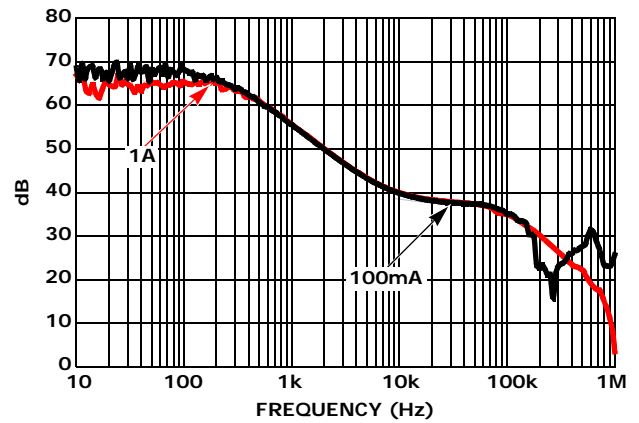


FIGURE 35. PSRR vs LOAD

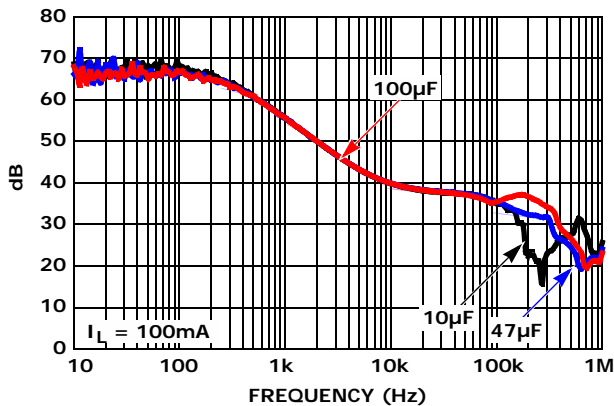


FIGURE 36. PSRR vs C_{OUT}

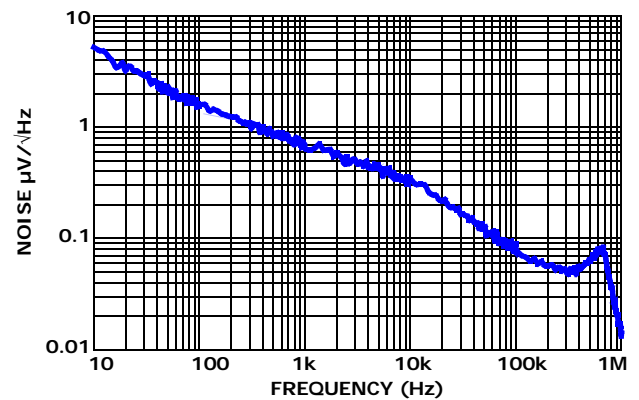


FIGURE 37. SPECTRAL NOISE DENSITY vs FREQUENCY

Functional Description

Input Voltage Requirements

Despite other output voltages offered, this family of LDOs is optimized for a true 2.5V to 1.8V conversion where the input supply can have a tolerance of as much as $\pm 10\%$ for conditions noted in the “Electrical Specifications” table on page 4. Minimum guaranteed input voltage is 2.2V, however, due to the nature of an LDO, V_{IN} must be some margin higher than the output voltage plus dropout at the maximum rated current of the application if active filtering (PSRR) is expected from V_{IN} to V_{OUT} . The dropout spec of this family of LDOs has been generously specified in order to allow applications to design for a level of efficiency that can accommodate the smaller outline package for those applications that cannot accommodate the profile of the TO220/263.

Enable Operation

The Enable turn-on threshold is typically 770mV with a hysteresis of 135mV. An internal pull-up or pull-down resistor is available upon request. As a result, this pin must not be left floating. This pin must be tied to V_{IN} if it is not used. A 1k Ω to 10k Ω pull-up resistor will be required for applications that use open collector or open drain outputs to control the Enable pin. The Enable pin may be connected directly to V_{IN} for applications that are always on.

Power-Good Operation

Applications not using this feature must connect this pin to ground. The PGOOD flag is an open-drain NMOS that can sink up to 10mA during a fault condition. The PGOOD pin requires an external pull-up resistor which is typically connected to the VOUT pin. The PGOOD pin should not be pulled up to a voltage source greater than V_{IN} . The PGOOD fault can be caused by the output voltage going below 84% of the nominal output voltage, or the current limit fault, or low input voltage. The PGOOD does not function during thermal shutdown. The PGOOD functions in shutdown.

Soft-Start Operation (Optional)

If the current limit for in-rush current is acceptable in the application, do not use this feature. The soft-start circuit controls the rate at which the output voltage comes up to regulation at power-up or LDO enable. A constant current charges an external soft-start capacitor. The external capacitor always gets discharged to ground pin potential at the beginning of start-up or enabling. The discharge rate is the RC time constant of R_{PD} and C_{SS} . See Figures 25 through 28 in the “Typical Operating Performance Curves” beginning on page 10. R_{PD} is the ON-resistance of the pull down MOSFET, M8. R_{PD} is 300 Ω typically.

The soft-start feature effectively reduces the in-rush current at power-up or LDO enable until V_{OUT} reaches regulation. The in-rush current can be an issue for applications that require large, external bulk

capacitances on V_{OUT} where high levels of charging current can be seen for a significant period of time. The in-rush currents can cause V_{IN} to drop below minimum which could cause V_{OUT} to shutdown. Figure 38 shows the relationship between in-rush current and C_{SS} with a C_{OUT} of 1000 μ F.

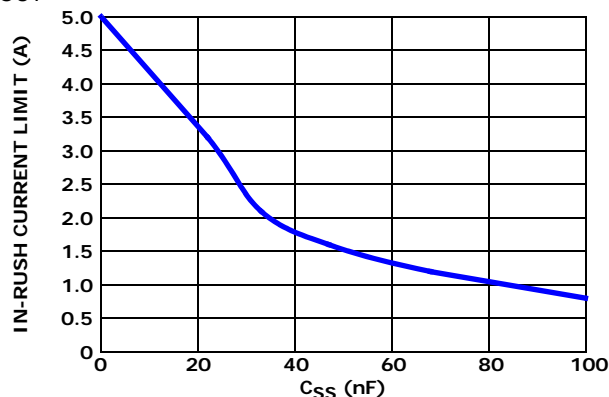


FIGURE 38. IN-RUSH CURRENT vs SOFT-START CAPACITANCE

Output Voltage Selection

An external resistor divider is used to scale the output voltage relative to the internal reference voltage. This voltage is then fed back to the error amplifier. The output voltage can be programmed to any level between 0.8V and 5V. An external resistor divider, R_3 and R_4 , is used to set the output voltage as shown in Equation 1. The recommended value for R_4 is 500 Ω to 1k Ω . R_3 is then chosen according to Equation 2:

$$V_{OUT} = 0.5V \times \left(\frac{R_3}{R_4} + 1 \right) \quad (\text{EQ. 1})$$

$$R_3 = R_4 \times \left(\frac{V_{OUT}}{0.5V} - 1 \right) \quad (\text{EQ. 2})$$

External Capacitor Requirements

External capacitors are required for proper operation. Careful attention must be paid to the layout guidelines and selection of capacitor type and value to ensure optimal performance.

OUTPUT CAPACITOR

The ISL80102, ISL80103 applies state-of-the-art internal compensation to keep selection of the output capacitor simple for the customer. Stable operation over full temperature, V_{IN} range, V_{OUT} range and load extremes are guaranteed for all capacitor types and values assuming a 10 μ F X5R/X7R is used for local bypass on V_{OUT} . This minimum capacitor must be connected to V_{OUT} and Ground pins of the LDO with PCB traces no longer than 0.5cm.

Lower cost Y5V and Z5U type ceramic capacitors are acceptable if the size of the capacitor is larger to compensate for the significantly lower tolerance over X5R/X7R types. Additional capacitors of any value in Ceramic, POSCAP or Alum/Tantalum Electrolytic types may be placed in parallel to improve PSRR at higher

frequencies and/or load transient AC output voltage tolerances.

INPUT CAPACITOR

The minimum input capacitor required for proper operation is 10µF having a ceramic dielectric. This minimum capacitor must be connected to V_{IN} and ground pins of the LDO with PCB traces no longer than 0.5cm.

Phase Boost Capacitor (Optional)

The ISL80102 and ISL80103 are designed to be stable with 10µF or larger ceramic capacitor.

Applications using the ADJ versions, may see improved performance with the addition of a small ceramic capacitor C_{PB} as shown in Figure 1 on page 3. The conditions where C_{PB} may be beneficial are: (1) $V_{OUT} > 1.5V$, (2) $C_{OUT} = 10\mu F$, and (3) tight AC voltage regulation band.

C_{PB} introduces phase lead with the product of R_3 and C_{PB} that results in increasing the bandwidth of the LDO. Typical $R_3 \times C_{PB}$ should be 4µs.

C_{PB} not recommended for $V_{OUT} < 1.5V$.

Current Limit Protection

The ISL80102, ISL80103 family of LDOs incorporates protection against overcurrent due to short, overload condition applied to the output and the in-rush current that occurs at start-up. The LDO performs as a constant current source when the output current exceeds the current limit threshold noted in the "Electrical Specifications" table on page 4. If the short or overload condition is removed from V_{OUT} , then the output returns to normal voltage mode regulation. In the event of an overload condition, the LDO might begin to cycle on and off due to the die temperature exceeding the thermal fault condition. The TO220/263 package will tolerate higher levels of power dissipation on the die which may never thermal cycle if the heatsink of this larger package can keep the die temperature below the specified typical thermal shutdown temperature.

Power Dissipation and Thermals

The junction temperature must not exceed the range specified in the "Recommended Operating Conditions

(Note 10)" on page 4. The power dissipation can be calculated by using Equation 3:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad (\text{EQ. 3})$$

The maximum allowable junction temperature, $T_{J(MAX)}$ and the maximum expected ambient temperature, $T_{A(MAX)}$ will determine the maximum allowable power dissipation as shown in Equation 4:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA} \quad (\text{EQ. 4})$$

Where θ_{JA} is the junction-to-ambient thermal resistance.

For safe operation, please make sure that power dissipation calculated in Equation 3, P_D be less than the maximum allowable power dissipation $P_{D(MAX)}$.

The DFN package uses the copper area on the PCB as a heat-sink. The EPAD of this package must be soldered to the copper plane (GND plane) for heat sinking. Figure 39 shows a curve for the θ_{JA} of the DFN package for different copper area sizes.

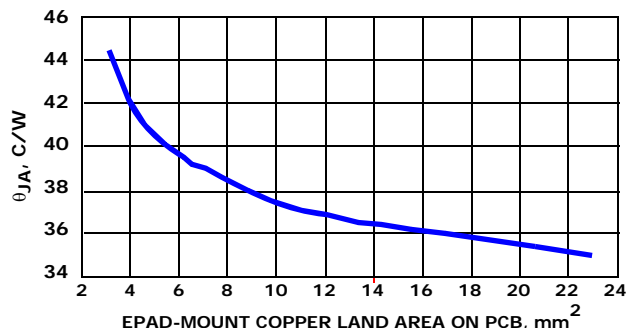


FIGURE 39. 3mmx3mm-10 PIN DFN ON 4-LAYER PCB WITH THERMAL VIAS θ_{JA} vs EPAD-MOUNT COPPER LAND AREA ON PCB

Thermal Fault Protection

In the event the die temperature exceeds typically +160°C, then the output of the LDO will shut down until the die temperature can cool down to typically +145°C. The level of power combined with the thermal impedance of the package (+48°C/W for DFN) will determine if the junction temperature exceeds the thermal shutdown temperature.

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Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
3/4/10	FN6660.1	<p>Corrected Features on page 1 as follows: -Changed bullet "• 185mV Dropout @ 3A, 125mV Dropout @ 2A" to "• Very Low 120mV Dropout at 3A" -Changed bullet "• 65dB Typical PSRR" to "• 62dB Typical PSRR" -Deleted 0.5% Initial VOUT Accuracy</p> <p>Modified Figure 1 and placed as Typical Application on Page 1.</p> <p>Moved Pinout to page 3 In "Block Diagram" on page 2, corrected resistor associated with M5 from R4 to R5</p> <p>Updated Block Diagram on page 2 as follows" - Added M8 from SS to ground.</p> <p>Updated Figure 1 on page 3 as follows: -Corrected Pin 6 from SS to IRSET -Removed Note 12 callout "Minimum cap on VIN and VOUT required for stability." Added Note "*CSS is optional. See Note 12 on Page 5." and "*** CPB is optional. See "Functional Description" on page 12 for more information."</p> <p>Added "The 1.5V, 3.3V and 5V fixed output voltages will be released in the future." to Note 3 on page 2.</p> <p>In "Thermal Information" on page 4, updated Theta JA from 45 to 48 per ASYD</p> <p>In "Soft-Start Operation (Optional)" on page 12: -Changed "The external capacitor always gets discharged to 0V at start-up of after coming out of a chip disable." to "The external capacitor always gets discharged to ground pin potential at start-up or enabling." -Changed "The soft-start function effectively limits the amount of in-rush current below the programmed current limit during start-up or an enable sequence to avoid an overcurrent fault condition." to "The soft-start feature effectively reduces the in-rush current at power-up or LDO enable until VOUT reaches regulation." -Added "See Figures 25 through 27 in the "Typical Operating Performance Curves" beginning on page 9." -Added "RPD is the on resistance of the pull down MOSFET, M8. RPD is 300Ohms typically."</p> <p>Added "Phase Boost Capacitor (CPB)" section on page 13.</p> <p>In "Typical Operating Performance" on page 11, revised figure "PSRR vs VIN" which had 3 curves with "Spectral Noise Density vs Frequency" which has one curve. Added "FIGURE 32. LOAD TRANSIENT 0A TO 3A, COUT = 10µF CERAMIC, NO CPB (ADJ VERSION)" and "FIGURE 33. LOAD TRANSIENT 1A TO 3A, COUT = 10µF CERAMIC, CPB = 1500pF (ADJ VERSION)"</p>
09/30/09	FN6660.0	Initial Release.

Products

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*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: [ISL80102](http://www.intersil.com/products), [ISL80103](http://www.intersil.com/products)

To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

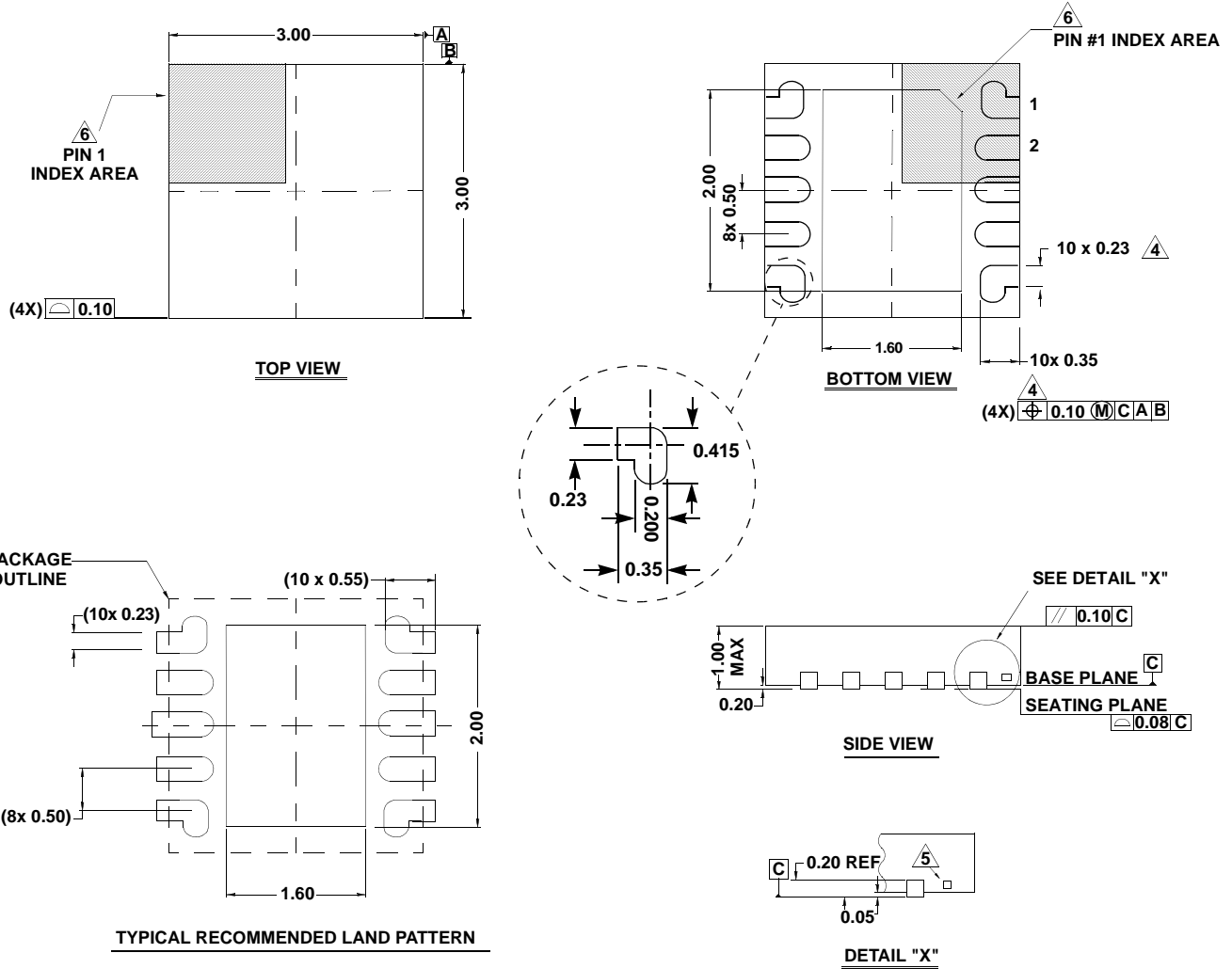
FITs are available from our website at <http://rel.intersil.com/reports/search.php>

Package Outline Drawing

L10.3x3

10 LEAD DUAL FLAT PACKAGE (DFN)

Rev 6, 09/09



NOTES:

1. Dimensions are in millimeters.
Dimensions in () for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Lead width applies to the metallized terminal and is measured between 0.18mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.